Amendments to the claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

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Claim 1 (previously presented): A shift register for shifting an input pulse in synchronization with a clock signal, the clock signal being smaller in amplitude than a driving voltage of a control circuit, comprising:

flip flops of a plurality of steps that output the input pulse in synchronization with the clock signal, said flip flops being divided into a plurality of blocks, each of the blocks including at least one of said flip flops; and

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a plurality of level shifters, one of the level shifters corresponding to each of the blocks, the level shifters for increasing the voltage of the clock signal and for applying the clock signal to each of said flip flops, said shift register transmitting the input pulse in synchronization with the clock signal,

wherein when one of the blocks does not require input of the clock signal, the corresponding level shifter is suspended at that point.

Claim 2 (original): The shift register as defined in claim 1, wherein at least one of said level shifters operates only when a corresponding block includes said flip flop requiring a clock signal input at that point.

Claim 3 (original): The shift register as defined in claim 1, wherein each of said level shifters operates only when a corresponding block includes said flip flop requiring a clock signal input at that point.

Claim 4 (original): The shift register as defined in claim 1, wherein a specific block of said blocks includes a set reset flip flop serving as said flip flop, said set reset flip flop being set in response to the clock signal, and

a specific level shifter corresponding to the specific block starts an operation at a start of a pulse input to the specific block and is suspended after setting said flip flop of a final step in the specific block.

Claim 5 (original): The shift register as defined in claim 4, wherein said specific block includes one of said flip flops, and

said specific level shifter starts an operation at a start of a pulse input to the specific block and is suspended at an end of the pulse input.

Claim 6 (original): The shift register as defined in claim 4, wherein said specific block includes a plurality of said flip flops, and

said specific level shifter operates during a pulse input to said specific block and during a pulse output of any one of said flip flops in a step except for the final step in the specific block.

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Claim 7 (original): The shift register as defined in claim 4, wherein said specific block includes a plurality of said flip flops, and

said specific level shifter includes a latch circuit which changes an output in response to a signal inputted to said specific block and an output signal of said flip flop in the final step of said specific block.

Claim 8 (original): The shift register as defined in any claim 1, wherein a specific block of said blocks includes a D flip flop as said flip flop, and

a specific level shifter corresponding to the specific block starts an operation at a start of a pulse input to the specific block and is suspended after a pulse output of said flip flop of a final step in the specific block.

Claim 9 (original): The shift register as defined in claim 8, wherein said specific block includes a plurality of said flip flops, and

said specific level shifter includes a latch circuit which changes an output in response to a signal inputted to said specific block and an output signal of said flip flop in the final step of said specific block.

Claim 10 (original): The shift register as defined in claim 1, wherein said level shifter includes a current-driven level shift section provided with an input switching element.

Claim 11 (original): The shift register as defined in claim 10, wherein said level shifter includes an input signal control section which suspends said level shifter by providing a signal at a level for interrupting said input switching element.

Claim 12 (original): The shift register as defined in claim 10, wherein said level shifter includes a power supply control section for suspending power supply to said level shift section so as to suspend said level shifter.

Claim 13 (original): The shift register as defined in claim 1, wherein each of said level shifters includes output stabilizing means.

Claim 14 (original): The shift register as defined in claim 13, wherein said level shifter includes a clock signal line for transmitting the clock signal, and a switch which is disposed between said clock signal line and said level shift section and is opened during suspension of said level shifter.

Claim 15 (original): An image display apparatus comprising data signal extracting means for extracting a data signal corresponding to each pixel from an image signal in synchronization with a clock signal, and data signal output means for outputting the data signal to each of the pixels, wherein said data signal extracting means includes said shift register defined in claim 1.

Claim 16 (original): An image display apparatus comprising:

a plurality of pixels disposed in a matrix form,

a plurality of data signal lines disposed for each row of said pixels,

a plurality of scanning lines disposed for each column of said pixels,

a scanning signal line driving circuit for successively applying a scanning signal with different timings to each of said scanning signal lines in synchronization with a first clock signal having a predetermined period, and

a data signal line driving circuit for extracting a data signal from an image signal applied to each of said pixels on said scanning line where the scanning signal is applied, and for outputting the data signal to said data signal lines, said image signal being successively applied in synchronization with a second clock signal having a predetermined period, said image signal indicating a display state of each of said pixels,

wherein at least one of said data signal line driving circuit and said scanning signal line driving circuit is provided with said shift register defined in claim 1, in which the first or second clock signal serves as said clock signal.

Claim 17 (original): The image display apparatus as defined in claim 16, wherein said data signal line driving circuit, said scanning signal line driving circuit, and said pixels are formed on the same substrate.

Claim 18 (original): The image display apparatus as defined in claim 16, wherein said data signal line driving circuit, said scanning signal line driving circuit, and said pixels include a switching element composed of a polycrystalline silicon thin film transistor.

Claim 19 (original): The image display apparatus as defined in claim 16, wherein said data signal line driving circuit, said scanning signal line driving circuit, and said pixels include a switching element manufactured at a process temperature of 600°C or less.

Claim 20 (previously presented): A shift register, in which a plurality of flip flops are connected, for transmitting an input pulse in synchronization with a clock signal, the clock signal being smaller in amplitude than a driving voltage of a control circuit, comprising:

a plurality of level shifters for level-shifting the clock signal, wherein at least one level shifter is provided for a predetermined number of said flip flops, the level shifters for increasing the voltage of the clock signal and for applying the clock signal to each of the flip flops,

wherein when one of the level shifters does not require input of the clock signal, the corresponding level shifter is suspended at that point.

Claim 21 (original): The shift resister as defined in claim 20, wherein at least one of a plurality of said level shifters suspends an operation.

Claim 22 (previously presented): The shift register as set forth in claim 1, wherein the level shifter operates in response to the input pulse that has been successively transmitted.

Claim 23 (previously presented): The shift register as set forth in claim 22, further comprising: a judging section, which identifies, based on the input pulse and an output signal, a level shifter which corresponds to blocks requiring no clock signal input, so as to control the input pulse into the level shifter.

Claim 24 (previously presented): The shift register as set forth in claim 20, wherein the level shifters operate in response to the input pulse that has been successively transmitted.

Claim 25 (previously presented): The shift register as set forth in claim 24, further comprising:

a judging section, which identifies, based on the input pulse and an output signal, a level shifter which corresponds to blocks requiring no clock signal input, so as to control the input pulse into the level shifter.

Claim 26 (new): A shift register for shifting an input pulse in synchronization with a clock signal, the clock signal being smaller in amplitude than a driving voltage of a control circuit, comprising:

flip flops of a plurality of steps that output the input pulse in synchronization with the clock signal, said flip flops being divided into a plurality of blocks, each of the blocks including at least one of said flip flops; and

a plurality of level shifters that operate by receiving the input pulse, one of the level shifters corresponding to each of the blocks, the level shifters for increasing the voltage of the clock signal and for applying the clock signal to each of said flip flops, said shift register transmitting the input pulse in synchronization with the clock signal,

wherein at least one of said plurality of level shifters corresponding to the block that does not at that point require an input of the clock signal is suspended by a reset in accordance with an output of the level shifter of one of the following blocks.

Claim 27 (new): A shift register, in which a plurality of flip flops are connected, for transmitting an input pulse in synchronization with a clock signal by using an output of each flip flop, the output being transmitted to the following flip flop, comprising:

a plurality of level shifters for level-shifting the clock signal, the level shifters operating by receiving the input pulse, wherein at least one level shifter is provided for a predetermined number of said flip flops, the level shifters for increasing the voltage of the clock signal and for applying the clock signal to each of the flip flops; and

each level shifter is reset in accordance with an output of one of the following level shifters.

Claim 28 (new): The shift register as defined in claim 1, wherein each level shifter operates by receiving, as the input pulse, an output of the flip flop at the previous step.

Claim 29 (new): The shift register as defined in claim 28, wherein each level shifter is suspended by receiving, as a reset signal, an output of the level shifter at two steps later.

Claim 30 (new): The shift register as defined in claim 27, wherein each level shifter operates by receiving, as the input pulse, an output of the flip flop at the previous step.

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Claim 31 (new): The shift register as defined in claim 30, wherein each level shifter is suspended by receiving, as a reset signal, an output of the level shifter at two steps later.